AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A method of synchronizing the frequency of a local clock of a digital data decoder with the frequency of a program clock, wherein the decoder includes clock adjustment hardware for adjusting the local clock frequency and a processor having a software program for adjusting the local clock frequency, the method comprising the steps of:

determining the difference between the local and program clock frequencies, then adjusting the frequency at which the local clock oscillates so that said difference approaches zero; including the steps of:

i) using the clock adjustment hardware to adjust the local clock frequency until a threshold condition occurs, and

after the threshold condition occurs, using the software program of the processor to adjust the local clock frequency.

2. (Currently Amended) A method according to Claim 1, wherein the local clock oscillates at the local clock frequency, the method further comprising the steps of:

maintaining a local clock value based on the oscillations of the local clock;

receiving program clock ~~time stamps~~ data at the decoder which specify ~~the program clock signals and~~ the frequency of the program clock;

maintaining a program clock value based on the program clock ~~signals~~ data received at the decoder;

determining if there is an absolute difference between the local clock value and the program clock value;

if there is an absolute difference between the local clock value and the program clock value, then adjusting the frequency at which the local clock oscillates so that said absolute difference approaches zero.

3. (Currently Amended) A method of synchronizing the frequency of a local clock of a digital data decoder with the frequency of a program clock, wherein the local clock oscillates at a local clock frequency, the method comprising the steps of:

determining the difference between the local and program clock frequencies, then adjusting the frequency at which the local clock oscillates so that said difference approaches zero;

maintaining a local clock value based on the oscillations of the local clock;

receiving program clock ~~time stamps~~ data at the decoder which specify ~~program clock signals and~~ the program clock frequency;

maintaining a program clock value based on the program clock ~~signals~~ data received at the decoder;

determining if there is an absolute difference between the local clock value and the program clock value;

if there is an absolute difference between the local clock value and the program clock value, then adjusting the frequency at which the local clock oscillates so that said absolute difference approaches zero;

wherein the decoder includes clock adjustment hardware for adjusting the local clock frequency and a processor having a software program for adjusting the local clock frequency, and wherein the step of adjusting the frequency of the local clock includes the steps of:

using the hardware to adjust the local clock frequency until a threshold condition occurs; and

after the threshold condition occurs, using the software program of the processor to adjust the local clock frequency.

4. (Original) A method according to Claim 3, wherein the threshold condition is a function of the difference between the local clock value and the program clock value.

5. (Currently Amended) A method according to Claim 3, wherein the step of using the software program of the processor to adjust the local clock frequency includes the steps of:

monitoring for the occurrence of the threshold condition; and

transmitting a signal to the processor when the threshold condition occurs.

6. (Cancelled)

7. (Currently Amended) A system for adjusting a local clock on a digital data decoder, wherein the clock oscillates at a local clock frequency, the system comprising:

~~means~~ a system time clock register for maintaining a local clock value based on the oscillations of the local clock;

means for receiving program clock ~~signals~~ data transmitted to the decoder that specify a program clock frequency;

~~means~~ a program clock register for maintaining a program clock value based on the clock ~~signals~~ data transmitted to the decoder;

means for determining if there is any difference between the local clock and the program clock frequencies;

~~means~~ a transport demultiplexer for determining if there is an absolute difference between the local clock value and the program clock value; and

means for adjusting the frequency at which the local clock oscillates, when there is a difference between the local clock and the program clock frequencies or an absolute difference between the local clock value and the program clock value, so that said difference approaches zero;

wherein the means for adjusting the frequency at which the local clock oscillates includes:

hardware for adjusting the local clock frequency until a threshold condition occurs; and

a processor having a software program for adjusting the local clock frequency after the threshold condition occurs.

8. (Previously Presented) A system according to Claim 7, wherein the threshold condition is a function of the difference between the local clock value and the program clock value.

9. (Original) A system according to Claim 7, wherein the processor is not used to adjust the local clock frequency until the threshold condition occurs.

10. (Currently Amended) A system according to Claim 7, said hardware includes:

~~means~~ a threshold register for monitoring for the occurrence of the threshold condition; and

means for transmitting a signal to the processor when the threshold condition occurs.

11. (Cancelled)

12. (Cancelled)

13. (Previously Presented) A system for synchronizing the frequency of a local clock of a digital data decoder with the frequency of a program clock, comprising:

means for determining if there is any difference between the local and program clock frequencies; and

means for adjusting the frequency at which the local clock oscillates, when there is a difference between the local clock and the program clock frequencies, so that said difference approaches zero, wherein the means for adjusting includes

i) hardware on the decoder for adjusting the local clock frequency until a threshold condition occurs, and

ii) a processor on the decoder and having a software program for adjusting the local clock frequency after the threshold condition occurs.

14. (Previously Presented) A system according to Claim 13, wherein the local clock has a local clock value and the program clock has a program clock value, and the threshold condition is a function of the difference between the local clock value and the program clock value.

15. (Currently Amended) A system according to Claim 13, wherein said hardware includes

~~means~~ a threshold register for monitoring for the occurrences of the threshold condition; and

means for transmitting a signal to the processor when the threshold condition occurs.